In the claims:

Please amend the claims as follows:

Please amend claims 6-7, 9, 23, 31-32, 39-40, 47-48, 53-56, 62-64 and 69-71 as follows.

1 -5 (Cancelled)

6. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to form a first metal element added region and a second metal element added region;

crystallizing the amorphous semiconductor film so that [a] crystal [growth proceeds] growths proceed in [a] crystal growth [direction] directions parallel to the insulating surface from the first metal element added region and the second metal element added region thereby to form a first crystalline portion and a second crystalline portion, respectively, in a crystalline semiconductor film; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island using only the first

crystalline portion while the second crystalline portion is not used to form the crystalline semiconductor island,

wherein the first metal element added region is away from the second metal element added region,

[whrerin] wherein carriers move in the crystalline semiconductor island in a carrier moving direction identical with the crystal growth direction,

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wherein the second metal element added region is located apart from the crystalline semiconductor island by a distance, and

wherein the first metal element added region has a length extending longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the first metal element added region.

7. (Currently Amended) A method according to claim 6, wherein [lengthes] lengths of the first metal element added region and the second element added region are set to 50% or more of a crystal growth distance.

8. (Previously Amended) A method according to claim 6, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

9. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

selectively providing a metal element being capable of promoting crystallization of the amorphous semiconductor film into at least a first region and a second region of the amorphous semiconductor film to form a first metal element added region and a second metal element added region, respectively;

crystallizing the amorphous semiconductor film so that [a] crystal [growthes] growths proceed in parallel to the insulating surface from each of the first metal element added region and the second metal element added region to form a first crystalline semiconductor region and a second crystalline semiconductor region, respectively; and

forming at least one active region of the semiconductor device in the first crystalline semiconductor region while the second crystalline semiconductor region is not used to form an active region of the semiconductor device,

wherein the first metal element added region is away from the second metal element added region.

10. (Previously Amended) A method according to claim 9,

wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

11. (Previously Amended) A method according to claim 9, wherein the metal element is provided by an ion implanting method.

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12. (Previously Amended) A method according to claim 9, wherein the metal element is provided by coating a solvent comprising the metal element.

13. (Cancelled)

14. (Previously Added) A method according to claim 9, wherein the amorphous semiconductor film comprises silicon.

15. (Previously Added) A method according to claim 9, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

16. (Previously Added) A method according to claim 9, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

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17. (Cancelled)

18. (Previously Added) A method according to claim 6, wherein the amorphous semiconductor film comprises silicon.

19. (Cancelled)

20. (Previously Added) A method according to claim 6, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

21. (Previously Added) A method according to claim 6,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

22. (Cancelled)

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23. (Currently Amended) A method according to claim 9, [further comprising controlling] wherein crystal growth state is controlled by [using] the second metal element added region.

24. (Previously Added) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to a selected region of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that a crystal growth proceeds in a direction parallel to the insulating surface from a metal element added region; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein the metal element added region has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the metal element added region.

25. (Previously Added) A method according to claim 24, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

26. (Previously Added) A method according to claim 24, wherein the metal element is provided by an ion implanting method.

27. (Previously Added) A method according to claim 24, wherein the metal element is provided by coating a solvent comprising the metal element.

28. (Previously Added) A method according to claim 24, wherein the amorphous semiconductor film comprises silicon.

29. (Previously Added) A method according to claim 24,

wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

30. (Previously Added) A method according to claim 24,

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wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

31. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two disconnected selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal [growthes] growths proceed in [a direction] directions parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands.

32. (Currently Amended) A method according to claim 31, wherein [lengthes] lengths of the metal element added regions are set to 50% or more of a crystal growth distance.

33. (Previously Added) A method according to claim 31, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

34. (Previously Added) A method according to claim 31, wherein the metal element is provided by an ion implanting method.

35. (Previously Added) A method according to claim 31,

wherein the metal element is provided by coating a solvent comprising the metal element.

36. (Previously Added) A method according to claim 31, wherein the amorphous semiconductor film comprises silicon.

37. (Previously Added) A method according to claim 31, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

38. (Previously Added) A method according to claim 31, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

39. (Currently Amended) A method according to claim 31,

[further comprising controlling] wherein crystal growth state [using a] is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

40. (Currently Amended) A method of manufacturing a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two disconnected selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal [growthes] growths proceed in [a direction] directions parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of a metal element added region, and

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands.

41. (Previously Added) A method according to claim 40, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

42. (Previously Added) A method according to claim 40, wherein the metal element is provided by an ion implanting method.

43. (Previously Added) A method according to claim 40, wherein the metal element is provided by coating a solvent comprising the metal element.

44. (Previously Added) A method according to claim 40, wherein the amorphous semiconductor film comprises silicon.

45. (Previously Added) A method according to claim 40, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

46. (Previously Added) A method according to claim 40, wherein the semiconductor device includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

47. (Currently Amended) A method according to claim 40, [further comprising controlling] wherein crystal growth state[using a] is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

48. (Currently Amended) A method of manufacturing [an invertor circuit] a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to a selected region of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that a crystal growth proceeds in a direction parallel to the insulating surface from a metal element added region; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein the metal element added region has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of the metal element added region, and

wherein the crystalline semiconductor island constitutes a TFT of an inverter circuit.

49. (Previously Added) A method according to claim 48, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

50. (Previously Added) A method according to claim 48, wherein the metal element is provided by an ion implanting method.

51. (Previously Added) A method according to claim 48, wherein the metal element is provided by coating a solvent comprising the metal element.

52. (Previously Added) A method according to claim 48, wherein the amorphous semiconductor film comprises silicon.

53. (Currently Amended) A method according to claim 48, wherein the [invertor] inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

54. (Currently Amended) A method according to claim 48, wherein the [invertor] inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

55. (Currently Amended) A method of manufacturing [an invertor circuit] a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two disconnected selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal [growthes] growths proceed in [a direction] directions parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands, and

wherein the crystalline semiconductor island constitutes a TFT of an inverter circuit.

56. (Currently Amended) A method according to claim 55, wherein [lengthes] lengths of the metal element added regions are set to 50% or more of a crystal growth distance.

57. (Previously Added) A method according to claim 55, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

58. (Previously Added) A method according to claim 55, wherein the metal element is provided by an ion implanting method.

59. (Previously Added) A method according to claim 55, wherein the metal element is provided by coating a solvent comprising the metal element.

60. (Previously Added) A method according to claim 55, wherein the amorphous semiconductor film comprises silicon.

61. (Currently Amended) A method according to claim 55, wherein the [invertor] inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

62. (Currently Amended) A method according to claim 55, wherein the [invertor] inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

63. (Currently Amended) A method according to claim 55, [further comprising controlling] wherein crystal growth state [using a] is controlled by the metal element added region that is not used to form crystalline semiconductor islands.

64. (Currently Amended) A method of manufacturing [an invertor circuit] a semiconductor device, said method comprising:

forming an amorphous semiconductor film on an insulating surface;

providing a metal element being capable of promoting crystallization of the amorphous semiconductor film to at least two disconnected selected regions of the amorphous semiconductor film;

crystallizing the amorphous semiconductor film to form a crystalline semiconductor film so that crystal [growthes]

growths proceed in [a direction] directions parallel to the insulating surface from metal element added regions; and

patterning the crystalline semiconductor film to form at least one crystalline semiconductor island,

wherein at least one of the metal element added regions has length extending 100μm or more longer from an end portion of the crystalline semiconductor island in a longitudinal direction of a metal element added region, and

wherein a portion of the crystalline semiconductor film formed by using one metal element added region is not used to form crystalline semiconductor islands, and

wherein the crystalline semiconductor island constitutes a TFT of an inverter circuit.

65. (Previously Added) A method according to claim 64, wherein the metal element comprises at least one selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

66. (Previously Added) A method according to claim 64, wherein the metal element is provided by an ion implanting method.

67. (Previously Added) A method according to claim 64,

wherein the metal element is provided by coating a solvent comprising the metal element.

68. (Previously Added) A method according to claim 64, wherein the amorphous semiconductor film comprises silicon.

69. (Currently Amended) A method according to claim 64, wherein the [invertor] inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not higher than 90 mV/dec while the p-channel thin film transistor has a second S value not higher than 100 mV/dec.

70. (Currently Amended) A method according to claim 64, wherein the [invertor] inverter circuit includes at least one selected from the group consisting of an n-channel thin film transistor and a p-channel thin film transistor,

wherein the n-channel thin film transistor has a first S value not lower than 75 mV/dec while the p-channel thin film transistor has a second S value not lower than 75 mV/dec.

71. (Currently Amended) A method according to claim 64,

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[further comprising controlling] wherein crystal growth state[using a] is controlled by the metal element added region that is not used to form crystalline semiconductor islands.